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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/024,025	12/21/2001	Michael Joachim Wolf	Q67574	4390

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EXAMINER

BHAT, ADITYA S

ART UNIT

PAPER NUMBER

2863

DATE MAILED: 08/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/024,025

Applicant(s)

WOLF ET AL. *W*

Examiner

Aditya S Bhat

Art Unit

2863

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☒ Claim(s) 1-4, 8, 9 and 11-13 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5-7, 10, 11-12 and 14-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Reynolds et al. (USPUB 20003/0126195).

With regards to claim 1, Reynolds et al. (USPUB 20003/0126195) teaches a method of synchronizing at least one receiver module, in particular a receiver module in a telecommunications network or in a network device of a telecommunications network, comprising the steps of:

- sending at least one first clock signal and a second clock signal to the at least one receiver module, (See figure 51)
- Sending at least one item of master-slave-status information about the at least one first clock signal and/or the second clock signal to the at least one receiver module, and (Page 36, Paragraph 0363)
- selecting as a function of the item of master-slave status information, at the at least one receiver module the first clock signal or the second clock signal as master synchronization signal for its synchronization. (Page 36, Paragraph 0364)

With regards to claim 11, Reynolds et al. (USPUB 20003/0126195) teaches a synchronisable receiver module in particular a receiver module in a telecommunications network or in a network device of a telecommunications network comprising:

receiving means for receiving at least one first clock signal and a second clock signal and comprising selection means for selecting the at least one first clock signal or the second clock signal as master synchronization signal for its synchronization, (Page 85, Paragraph 0814)

wherein the receiving means are designed to receive at least one item of master-slave status information about the at least one first clock signal and/or the second clock signal, and wherein the selection means are designed such that as a

Art Unit: 2863

function of the item of master-slave-status information the receiver module can select the at least one first clock signal or the second clock signal as master synchronization signal for its synchronization. (Page 85, Paragraph 0814)

With regards to claim 12, Reynolds et al. (USPUB 20003/0126195) teaches a clock generator module, in particular a clock generator module in a telecommunications network or in a network device of a telecommunications network, for synchronizing at least one receiver module,

with clock generation means for generating at least one first clock signal (See figure 51 and Page 5 Paragraph 0106) and with

transmitting means for transmitting the at least one first clock signal to the at least one receiver module, wherein the transmitting means are designed to transmit at least one item of master-slave-status information about the at least one clock signal so that as a function of the master-slave-status information the at least one receiver module can select the at least one first clock signal or a second clock signal as master synchronization signal for its synchronization. (Page 18, Paragraph 0211)

With regards to claim 2, Reynolds et al. (USPUB 20003/0126195) teaches at least one first clock signal or the second clock signal is defined as a preferred master synchronization signal, and wherein the at least one receiver module selects as master synchronization signal the at least one first clock signal or second clock signal which is defined as preferred master synchronization signal when the at least one first clock signal or second clock signal to be selected as master synchronization signal cannot be detected on the basis of the at least one item of master-slave-status information, in particular because the item of master slave-status information is not sent, or is faultily sent, to the at least one receiver module, or the at least one item of master-slave-status information identifies both the at least one clock signal and the second clock signal as master synchronization signal. (See figure 51)

With regards to claim 3, Reynolds et al. (USPUB 20003/0126195) teaches at least one first clock signal is generated by a first clock generator module and the second clock signal is generated by a second clock generator module, wherein at least the first clock generator module sends the second clock generator module a synchronization signal provided in particular for its synchronization, and wherein the at least one item of master-slave-status information defines the first clock signal as master synchronization signal for such time as the second clock generator module receives the synchronization signal.

With regards to claim 5, Reynolds et al. (USPUB 20003/0126195) teaches at least one item of master-slave-status information is contained at least partially in the first clock signal and/or at least partially in the second clock signal. (See figure 12A)

With regards to claim 6, Reynolds et al. (USPUB 20003/0126195) teaches at least one first clock signal is sent on a first clock line, and the second clock signal on a second clock line, to the at least one receiver module. (See figure 51)

With regards to claim 7, Reynolds et al. (USPUB 20003/0126195) teaches at least one first clock signal and/or the second clock signal and/or an item of control

Art Unit: 2863

information assigned thereto contains at least one item of source information from which the at least one receiver module can determine the source from which the at least one first clock signal and the second clock signal emanates, in particular that the first clock generator module and the second clock generator module add the respective items of source information, by which they are identified, to the at least one first clock signal and the second clock signal, respectively. (See figure 51)

With regards to claim 10, Reynolds et al. (USPUB 20003/0126195) teaches with a first delay means, the at least one first receiver module delays the at least one first clock signal by a predetermined first delay time which in particular corresponds to a maximum expected propagation time difference between the at least one first clock signal and the second clock signal, wherein the at least one receiver module delays the second clock signal in a second delay means, wherein the receiver module determines a phase difference between the at least one first clock signal and the second clock signal, and wherein the receiver module adapts the phase of the second clock signal to the phase of the first clock signal by adjusting the second delay means so that the at least one receiver module can extract the at least one first clock signal and the second clock signal in-phase from the first delay means and from the second delay means respectively. (See figure 51)

With regards to claim 14, Reynolds et al. (USPUB 20003/0126195) teaches a program code, which can be executed by a control, means of a network device, in particular by a control means on a console of a network device for a transmission network with a synchronous digital hierarchy. (Page 70, Paragraph 0675)

With regards to claim 15 and 18, Reynolds et al. (USPUB 20003/0126195) teaches a program code, which can be executed by a control, means of a network device, in particular by a control means on a console of a network device for a transmission network with a synchronous digital hierarchy. (Page 70, Paragraph 0675)

With regards to claim 16, Reynolds et al. (USPUB 20003/0126195) teaches a storage medium storing module (See figure 12A)

With regards to claim 17 and 19, Reynolds et al. (USPUB 20003/0126195) teaches a network device, for a transmission network with a synchronous digital hierarchy, with at least one receiver module (Page 85, Paragraph 0814)

Claim Objections

Claims 1-4, 8-9, and 11-13 are objected to because of the following informalities:

Synchronisation is misspelled. The correct spelling is Synchronization. Appropriate correction is required.

The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign

Art Unit: 2863

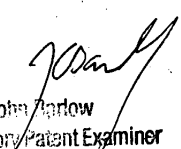
document and are replete with grammatical and idiomatic errors. Applicant is urged to reformat the claims in order to clearly show the individual steps and components of the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aditya S Bhat whose telephone number is 703-308-0332. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 703-308-3126. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-5841 for regular communications and 703-308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Aditya S.Bhat
August 8, 2003


John Barlow
Supervisory Patent Examiner
Technology Center 2800